Amendments to the Claims

1. (*Currently Amended*) Method for fabrication of a memory cell, for storing at least one bit, on a semiconductor substrate ~~(2)~~, comprising on said substrate ~~(2)~~ a first floating gate stack (A), a second floating gate stack (B) and an intermediate access gate ~~(AG)~~, said first and second floating gate stacks ~~(A, B)~~ comprising a first gate oxide layer ~~(4)~~, a floating gate ~~(FG)~~, a control gate ~~(CG; CGl, CGu)~~, an interpoly dielectric layer ~~(8)~~, a capping layer ~~(6)~~ and side-wall spacers ~~(10)~~, said first gate oxide layer ~~(4)~~ being located on said substrate ~~(2)~~, said floating gate ~~(FG)~~ being on top of said first gate oxide layer ~~(4)~~, said interpoly dielectric layer ~~(8)~~ being on top of said floating gate ~~(FG)~~, said control gate ~~(CG; CGl, CGu)~~ being on top of said interpoly dielectric layer (8), said capping layer ~~(6)~~ being on top of said control gate ~~(CG; CGl, CGu)~~, said memory cell further comprising source and drain contacts ~~(22)~~, said method of fabrication comprising:

~~[[-]]~~ defining said first and second floating gate stacks ~~(A, B)~~ in the same processing steps to have substantially equal heights;

~~[[-]]~~ depositing a poly-Si layer ~~(12)~~ over said first and second floating gate stacks ~~(A, B)~~, said poly-Si layer being deposited in between said first and second floating gate stacks ~~(A, B)~~ in a thickness equal to or larger than the height of said first and second floating gate stacks ~~(A, B)~~;

~~[[-]]~~ planarizing said poly-Si layer ~~(12)~~ by chemical mechanical polishing to obtain a planarized poly-Si layer ~~(14)~~, using said capping layer ~~(6)~~ of said first and second floating gate stacks ~~(A, B)~~ as a polish stop layer;

~~[[-]]~~ defining said intermediate access gate ~~(AG)~~ in said planarized poly-Si layer ~~(14)~~ by a masking step with an access gate mask ~~(20)~~ over said planarized poly-Si layer between said first and second floating gate stacks ~~(A, B)~~ and an etching step for poly-Si.

2. (*Currently Amended*) Method for fabrication of a memory cell, according to claim 1, characterized by:

~~[[-]]~~ forming on top of said intermediate access gate ~~(AG)~~ a first self-aligned silicide area ~~(28)~~ and on top of said source and drain contacts ~~(22)~~ a second self-aligned silicide area ~~(26)~~;

~~[[-]]~~ forming on said second self-aligned silicide area ~~(26)~~ a local interconnect ~~(30)~~;

~~[[-]]~~ depositing on top of said local interconnect ~~(30)~~, said first self-aligned silicide area ~~(28)~~, and said capping layer ~~(6)~~ a pre-metal dielectric layer ~~(32)~~;

~~[[-]]~~ forming a contact opening ~~(CO)~~ in said pre-metal dielectric layer ~~(32)~~ to said local interconnect ~~(30)~~;

~~[[-]]~~ filling said contact opening ~~(CO)~~ with a metal contact ~~(34)~~ to said local interconnect ~~(30)~~; and

~~[[-]]~~ defining on top of said pre-metal dielectric layer ~~(32)~~ at least one metal line as a bit-line ~~(40)~~.

3. (*Currently Amended*) Method for fabrication of a memory cell, according to claim 1, characterized by:

~~[[-]]~~ forming on top of said intermediate access gate ~~(AG)~~ a first self-aligned silicide area ~~(28)~~ and on top of said source and drain contacts ~~(22)~~ a second self-aligned silicide area ~~(26)~~;

~~[[-]]~~ depositing on top of said second self-aligned silicide area ~~(26)~~, said first self-aligned silicide area ~~(28)~~ and said capping layer ~~(6)~~ a pre-metal dielectric layer ~~(32)~~;

~~[[-]]~~ forming a contact opening ~~(CO)~~ in said pre-metal dielectric layer ~~(32)~~ to said second self-aligned silicide area ~~(26)~~;

~~[[-]]~~ filling said contact opening ~~(CO)~~ with a metal contact ~~(50)~~ to said second self-aligned silicide area ~~(26)~~; and

~~[[-]]~~ defining on top of said pre-metal dielectric layer ~~(32)~~ at least one metal line as a bit-line ~~(41)~~, said bit-line ~~(41)~~ being slanted.

4. (*Currently Amended*) Method for fabrication of a memory cell, ~~according to claim 1 or 3,~~ according to claim 1, characterized by:

~~[[-]]~~ forming on top of said intermediate access gate ~~(AG)~~ a first self-aligned silicide area ~~(28)~~ and on top of said source and drain contacts ~~(22)~~ a second self-aligned silicide area ~~(26)~~;

~~[[-]]~~ depositing on top of said second self-aligned silicide area ~~(26)~~, said first self-aligned silicide area ~~(28)~~ and said capping layer ~~(6)~~ a pre-metal dielectric layer ~~(32)~~;

[[-]] forming a contact opening ~~(CO)~~ in said pre-metal dielectric layer ~~(32)~~ to said second self-aligned silicide area ~~(26)~~;

[[-]] filling said contact opening ~~(CO)~~ with a contact ~~(50)~~ to said second self-aligned silicide area ~~(26)~~; and

[[-]] defining on top of said pre-metal dielectric layer ~~(32)~~ in a first metal level ~~(metal-1)~~ said bit-line ~~(42)~~ for connecting to said contact opening (CO), said bit-line ~~(42)~~ being slanted.

5. (*Currently Amended*) Method for fabrication of a memory cell, according to claim 4, characterized by:

[[-]] forming on top of said intermediate access gate ~~(AG)~~ a first self-aligned silicide area ~~(28)~~ and on top of said source and drain contacts ~~(22)~~ a second self-aligned silicide area ~~(26)~~;

[[-]] depositing on top of said second self-aligned silicide area ~~(26)~~, said first self-aligned silicide area ~~(28)~~, and said capping layer ~~(6)~~ a pre-metal dielectric layer ~~(32)~~;

[[-]] forming a contact opening ~~(CO)~~ in said pre-metal dielectric layer ~~(32)~~ to said second self-aligned silicide area ~~(26)~~;

[[-]] filling said contact opening ~~(CO)~~ with a contact ~~(52)~~ to said second self-aligned silicide area ~~(26)~~; and

[[-]] defining on top of said pre-metal dielectric layer ~~(32)~~ in said first metal level ~~(metal-1)~~ a landing pad ~~(49)~~ on top of said contact ~~(52)~~ for connecting to said contact opening ~~(CO)~~ by means of:

[[-]] depositing an intermetal dielectric layer,

[[-]] forming a further contact opening as a via opening in said intermetal dielectric layer,

[[-]] filling said via opening with a contact ~~(48)~~ acting as a via, and

[[-]] defining in a second metal level ~~(metal-2)~~ a further slanted bit-line ~~(43)~~ on top of said intermetal dielectric layer for connection to said contact ~~(48)~~ acting as a via, said contact ~~(48)~~ acting as a via being connected to said landing pad ~~(49)~~.

6. (*Currently Amended*) Method for fabrication of a memory cell, ~~according to any of the preceding claims,~~ according to claim 1, characterized by:

[[-]] said floating gate FG consisting of a trapping medium,

[[-]] said trapping medium comprising an ONO layer stack, an oxygen-rich silicon layer, or a silicon dioxide layer comprising silicon nanocrystals dispersed therein.

7. (*Currently Amended*) Memory cell, for storing at least one bit, on a semiconductor substrate ~~(2)~~, comprising on said substrate ~~(2)~~ a first floating gate stack ~~(A)~~, a second floating gate stack ~~(B)~~ and an intermediate access gate ~~(AG)~~, said first and second floating gate stacks ~~(A, B)~~ comprising a first gate oxide layer ~~(4)~~, a floating gate ~~(FG)~~, a control gate ~~(CG; CGl, CGu)~~, an interpoly dielectric layer ~~(8)~~, a capping layer ~~(6)~~ and sidewall spacers ~~(10)~~, said first gate oxide layer ~~(4)~~ being located on said substrate ~~(2)~~, said floating gate ~~(FG)~~ being on top of said first gate oxide layer ~~(4)~~, said interpoly dielectric layer ~~(8)~~ being on top of said floating gate ~~(FG)~~, said control gate ~~(CG; CGl, CGu)~~ being on top of said interpoly dielectric layer ~~(8)~~, said capping layer ~~(6)~~ being on top of said control gate ~~(CG; CGl, CGu)~~, said memory cell further comprising source and drain contacts ~~(22)~~, characterized in that

[[-]] said first and second floating gate stacks ~~(A, B)~~ have substantially equal heights;

[[-]] said intermediate access gate ~~(AG)~~ comprises a planarized poly-Si layer ~~(14)~~ in between said first and second floating gate stacks ~~(A, B)~~.

8. (*Currently Amended*) Array of memory cells, characterized in that said array comprises at least two adjacent memory cells ~~(C, D)~~ according to claim 7.

9. (*Currently Amended*) Array of memory cells according to claim 8, characterized in that

[[-]] said at least two adjacent memory cells ~~(C, D)~~ are arranged in a virtual ground arrangement; and

[[-]] in said virtual ground arrangement a bit-line is a metal line ~~(40; 41; 42; 43)~~; said bit-line being connected to said second self-aligned silicide area ~~(26)~~ by a contact ~~(30; 34; 50; 50; 48, 49, 52)~~ in said contact opening ~~(CO)~~.

10. (*Currently Amended*) Array of memory cells according to claim 9, characterized in that in said array of memory cells at least two memory cells connect to said contact opening ~~(CO)~~ for said bit-line ~~(40; 41; 42, 43)~~.

11. (*Original*) Array of memory cells according to claim 8, characterized in that said at least two memory cells are programmed selectively by Source-Side-Injection, and said at least two memory cells are erased by Fowler-Nordheim Tunneling or by Hot Hole Injection.

12. . (*Original*) Array of memory cells according to claim 8, characterized in that said at least two memory cells are programmed selectively by Fowler-Nordheim Tunneling, and said at least two memory cells are erased by Fowler-Nordheim Tunneling or by Hot Hole Injection.

13. (*Currently Amended*) Array of compact memory cells ~~according to claim 10 or 11 or 12~~, according to claim 10, characterized in that said bit-line ~~(41)~~ is slanted and connected to memory cells, which are not ~~"horizontally"~~ horizontally neighboring cells having the same control gate ~~(CGu, CGl)~~.

14. (*Currently Amended*) Array of compact memory cells ~~according to claim 10 or 11 or 12~~, according to claim 10, characterized in that

~~[[-]]~~ in a first metal deposition process level (metal-1) said bit-line as a metal-1 bit-line ~~(42)~~ comprises a plurality of first line parts ~~(44)~~ running in a direction parallel to said active lines and a plurality of second line parts ~~(45)~~, each of said first line parts ~~(44)~~ being formed on top of one of said contacts ~~(50)~~, said second line parts ~~(45)~~ being formed in between said contacts ~~(50)~~, and

~~[[-]]~~ in a second metal deposition process level (metal-2)said bit-line as a metal-2 bit-line ~~(43)~~ comprises a plurality of first line parts ~~(44)~~ running in a direction parallel to said active lines and a plurality of second line parts ~~(45)~~, each of said first line parts ~~(44)~~ being formed on top of one of said contacts ~~(48)~~ acting as a via, said second line parts ~~(45)~~ being formed in between said contacts ~~(48)~~ acting as a via;

~~[[ ]]~~ said bit-line ~~(42, 43)~~ running step-wise for connecting to memory cells, which are not ~~"horizontally"~~ horizontally neighboring cells having the same control gate ~~(CGu, CGl)~~, with each of said second line parts ~~(45)~~ running in a direction perpendicular to said active lines or running in a slant direction relative to said active lines.

15. (*Original*) Semiconductor device comprising at least one memory cell according to claim 7.